
CS82L44 Schematic and Layout Guidelines

Introduction

This document describes the schematic and layout guidelines for the CS82L44 Four-Channel AFE with Sensor Timing Generation and LVDS/CMOS Data Output.

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1 General Board Considerations

- Use controlled 50Ω characteristic impedance for digital signals unless stated otherwise.

2 Layout Guidelines

2.1 Note 1: Device Decoupling

- Place decoupling capacitors close to device on same side of PCB.
- VDD_A and VDD_IO decoupling take 1st priority (Figure 1).

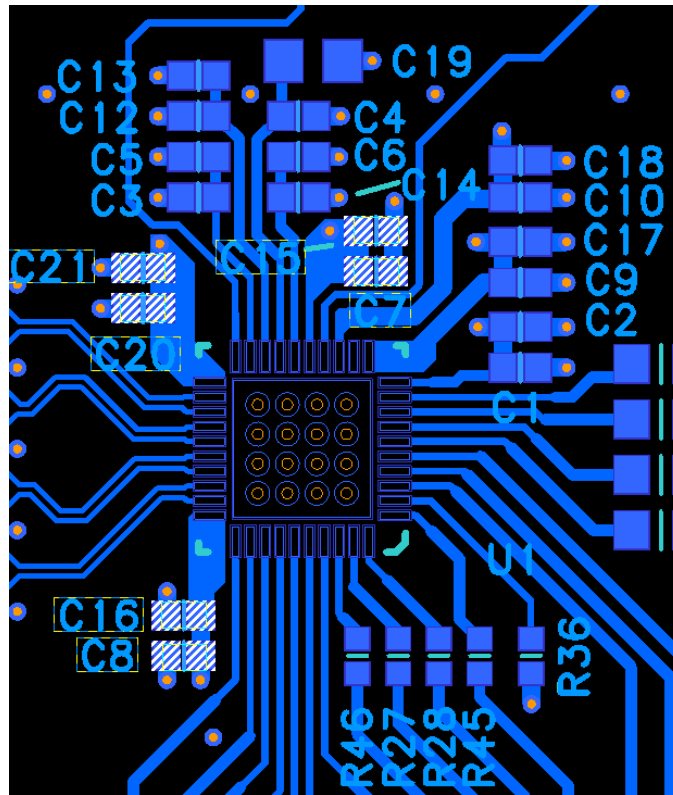


Figure 1 - Device Decoupling with VDD_A and VDD_IO decoupling highlighted

2.2 Note 2: Source Termination

- Use termination when system trace lengths justify it.
- Place 33R termination close to device.
- Termination takes second priority to decoupling capacitor placement.

2.3 Note 3: LVDS Controlled Impedance

- Use 100Ω controlled differential impedance for LVDS pairs.

2.4 Note 4: LVDS Intra-Pair Skew

- Keep intra-pair skew between PCB traces (DOUTx_N-DOUTx_P) to a maximum of 10ps.

2.5 Note 5: LVDS Inter-Pair Skew

- Maximum PCB trace inter-pair skew (DOUTx_P/N-DOUTy_P/N) should be calculated based on the LVDS data output switching specifications in the CS82L44 datasheet and the LVDS receiver timing specifications.

2.6 Note 6: Ground Paddle

Connect the device's ground paddle to the nearest ground plane with 0.3mm diameter vias on a 4x4, 0.8mm grid.

3 Revision History

Revision History	
Revision	Changes
1.0 JUL 2024	Initial version.

Contacting Cirrus Logic Support

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